Standalone Single Phase DC-AC Inverter with FPGA-based Pulse Modulated Generator Unit

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***Abstract*— This paper presents the design of a pulse modulation signal generator using a Field Programmable Gate Array (FPGA) to control the power switch devices used in an inverter that are arranged in full bridge configuration. A single-phase inverter is designed for stand-alone operation mode in renewable energy-based power supply system. FPGA is an electronic device that works digitally and has the advantage of being able to work at high frequency and high concurrent computing capability. The modulated pulse signal is generated by comparing a sinusoidal wave and triangular wave generated digitally using the Look-Up Table (LUT) method to retrieve an amount of voltage data at some points of sampling. The data obtained is then stored in the FPGA internal memory. To test the hardware, an LC filters are used to reduce harmonic caused by the switching process and produce pure sinusoidal output quality. System validation is made using two methods, i.e. SPICE simulation and testing on the real inverter unit. Total harmonic distortion (THD) of the inverter hardware is measured and analyzed.**

Keywords—Power Electronic, Single Phase Inverter, FPGA, LC Filter, SPWM, Look Up Table (LUT).

I. INTRODUCTION

Electric power system generations that use fossil fuels are not only costly but also unfriendly to environment. In any cases, power system distribution cannot reach some rural areas. The use of solar cell or photovoltaic panels, wind energy, and hydro power can be implemented to generate power for the rural areas, which can be designed for small scale or micro grid scale [1]. Most of renewable electric powers produce direct current (DC). Therefore, an inverter DC-AC is used as a power equipment that converts electric power from DC power to alternating current (AC) power. This conversion is made, since the voltage waveform standard used in home or power consumer installation is AC voltage [2].

Some research works have been done to improve the inverter performance including reducing design cost by miniaturizing the inverter's components and module size. Increasing switching frequency can reduce the module and component sizes including the power filter components and can improve also the efficiency [2, 3, 4, 5]. However, switching frequency increase must comply with the specification of the power semiconductor devices. This should be made to avoid switching loses and to improve the aging condition of the power devices.

There are many techniques to generate AC inverting output signal of the inverter. One of them is a sinusoidal-based pulse width modulation (SPWM) technique, which is applied to power switching device, mostly a MOSFET device. The SPWM control signal is generated by comparing two periodic signals, i.e. a saw tooth signal having fixed frequency called modulating or carrier frequency and a sinusoidal having fixed frequency equal to grid frequency. In general, the modulating frequency is set higher or much higher than the grid frequency. The SPWM control signal can also generated using other techniques such as a pre-sampling time for the on-time (T_{on}) and off-time (T_{off}) of the SPWM signal [8][9]. However, this technique requires a pre experimental measurements, and must be repeated each time a new modulation frequency or modulation index will be set to the SPWM generator unit.

In this paper, a Look-Up Table (LUT) method is used to take sine wave sampling points during a single cycle period. The number of stored sample points is determined to fit the signal generation, which satisfies acceptable waveforms. The sample points are then used to generate the saw tooth and the sine wave signals [5, 6]. A comparator is then used to compare the sine wave and the saw tooth signal, where the comparator output signals are used to set the condition of the power switching devices in the inverter circuit.

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This paper is part of our research project to design a sustainable renewable-energy-based power supply system with a special feature of DC power lines. The architecture of the overall system is presented in Fig. 1. The domain of this paper covers only the DC-AC inverter unit that provides power for AC power line with 220VAC at 50 Hz frequency as shown in the figure. The complete system itself consists of a maximum power point tracking (MPPT) unit, SCR-based rectifier, DC-DC converter, charge controller and the inverter DC-AC. The system is controlled by an integrated electronic control unit that will be implemented using a complex programmable logic device (CPLD) or a field programmable gate array (FPGA). For optimal mass production cost, the control unit can be potentially implemented in an application-specific integrated circuit (ASIC) or a single system-on-chip device.

Certainly, the control unit for the inverter can be implemented using a microcontroller unit. However, since this project aims to implement all control unit that fit in a single low cost CPLD or FPGA device for optimal production cost purpose, this paper presents our research outcome that make use of the FPGA device to generate the SPWM signal for the inverter.

The FPGA device is capable to work at higher frequency (in hundred MHz), flexible or reconfigurable and can work in concurrent mode [5, 6, 7]. The FPGA device consists of logic elements that can be programmed using hardware description language (HDL) programming. It inherently consists of programmable look-up-table (LUT) logic block. Hence, programming LUT logics in the FPGA device is simple.

This paper presents the single-phase inverter with LC power passive filter. The LC filter is used to damp the total harmonic distortion (THD) of the inverter output voltage. Higher switching frequency enables us to use lower inductance and capacitance values of the filter's L-C components [11, 12]. Certainly, there are many other advanced power passive filters that can be used.

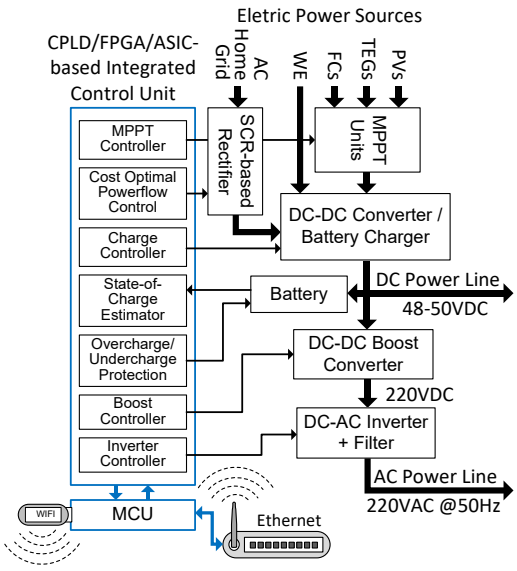


Fig. 1. The overall micro/home grid scale power supply equipment.

However, this paper is not focused on that issue and does not deliver contribution to the paper.

The main contribution of this paper is the use of LUT-based logic block to implement the SPWM signal generator block on an FPGA device, where this block is used to generate AC power signal by the inverter unit. Any existing silicon compiler tools can be used to optimize the LUT-based logic design. Since the number of logic elements (LEs) required to build the SPWM generator is very low, only 107 LEs, then when our unit block will be implemented in a single intellectual property (IP) core, it will consume less power.

II. The System Description

The block diagram of a full bridge inverter topology is presented in Fig. 2. The inverter topology produces AC voltage by periodically exchange the activation of power devices M1, M2 and M3, M4. Battery module is used to store energy. Auxiliary power supply is used to supply power for the FPGA device (3.3 V_{DC}) dan MOSFET driver (18 V_{DC}). The PV modules together with an MPPT unit and battery charger will provide input power for the inverter.

The FPGA unit as the SPWM pulse generator will control the switching mechanism of the switching devices (MOSFETs M_1, M_2, M_3 and M_4). The pulses generated by the FPGA have low voltage level, i.e. 3.3 V_{DC}. The MOSFET driver will increase the voltage level to be 30V_{DC} or any higher voltage according to the specification of the MOSFET.

The waveform of the inverter output voltage is still in AC with SPWM waveform, which certainly contains many harmonic distortions. A power passive filter, i.e, LC Filter as shown in Fig. 2 is used to damp the THD of the inverter's output voltage. A transformer is used to step-up the AC voltage amplitude to be 220 V.

III. FPGA-Based SPWM Signal Generation

FPGA is a reconfigurable logic platform. Concurrent logic processing can be implemented on an FPGA. The SPWM signal generator is digitally implemented using a Look-Up Table (LUT) method. The LUT consists of 64 slots to store 7-bit sine and triangle (sawtooth) waveform data. Selected number of sample points is made in accordance with the number of sampling time. The larger the sampling time, the smoother digital waveform generated by SPWM signal generator [2, 14].

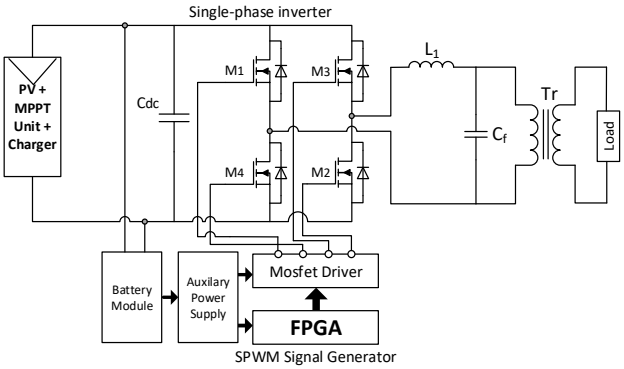


Fig. 2. Block digram of the DC-AC inverter with an LC power filter.

Fig. 3(a) presents the digital waveforms of the saw tooth signal and the sine wave signal.

$$V_{sr}(t) = V_m sin\frac{2\pi t}{n_s} \quad (1)$$

$$V_{s\Delta}(t) = V_m \frac{2t}{n_\Delta} \quad \text{for } (0 < t < \frac{n_\Delta}{2}) \quad (2)$$

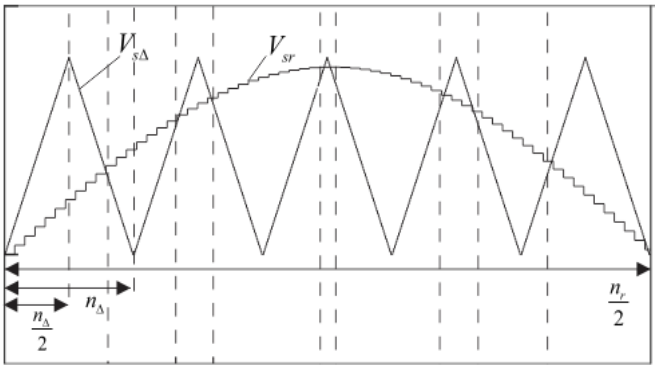
$$V_{s\Delta}(t) = V_m - \left(V_m \frac{2t}{n_\Delta}\right) \quad \text{for } (\frac{n_\Delta}{2} < t < n_\Delta) \quad (3)$$

Fig. 3(b) presents the block diagram of the SPWM signal generator, which is implemented on the FPGA device. The FPGA board is clocked with 50 MHz. The sine wave block is used to generate sine signal (V_{sr}) and triangle wave block is to generate sawtooth signal ($V_{s\Delta}$). Comparator block will compare the sine and saw tooth signal to generate the expected SPWM signal ($V_{s\Delta} < V_{sr} = 1$) using the following modulation index formula (m_a) [2].

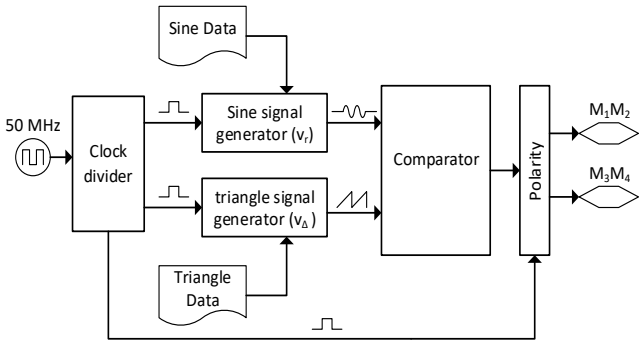
$$m_a = \frac{V_{sr}}{V_{s\Delta}} \quad (4)$$

IV. The LC Passive Power Filter

The LC filter is a passive filter that consists of several passive components L and C, as shown in Fig. 4. The LC filter design aims to produce passive filtering that can minimize harmonic interference. It is therefore very important to determine correct parameters when designing an LC filter.



(a)



(b)

Fig. 3. (a) Generated saw tooth and sine wave signal by the FPGA device. (b) Block diagram of the SPWM signal generator implemented on FPGA.

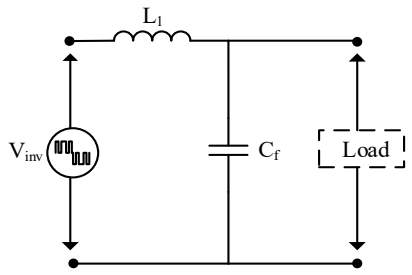


Fig. 4. LC filter circuit.

The filter resonance occurs due to the harmonic current in the inverter. Therefore, the determination of the value of the inductor L_1 mounted on the inverter side depends on the magnitude of the current ripple value and the switching frequency of inverter (f_{sw}). In general, the current ripple value (ΔI) must be over 20% and under 40% [12].

$$\omega_s = 2\pi f_{sw} \quad (5)$$

The term ω_s is the resonance frequency, and f_{sw} is the switching frequency to generate a single period of the triangle or sawtooth signal. Therefore, the higher the frequency of f_{sw}, the larger the number of triangle waveform generated in a single 20-ms-period.

The quantity α as a function of f_{sw} for the maximum ripple current is 20% and 40% on the condition that it must satisfy equation 6 [12]. Where ω_o is the fundamental frequency and ω_c is the cut-off frequency angle [12].

$$\omega_c > \frac{\omega_o}{\sqrt{\alpha}} \quad (6)$$

The determination of the factor k with index modulation ($m = 0.95$) generally has a standard value of $k = 15$. The resonance frequency f_c can thus be determined by the equation.

$$f_c < \frac{f_{sw}}{k} \quad (7)$$

or

$$f_c = \frac{1}{\sqrt{L_1 C_f}} \quad (8)$$

However, if $m < 0{,}95$, this can be determined from the equation.

$$\omega_c > \frac{1}{k}\omega_s \quad with \quad k > 15 \quad (9)$$

The values for inductor (L_1) and capacitor (C_f) can be obtained from the following equation, i.e.

$$L_1 = \frac{R_{lm}}{\omega_o}\sqrt{\alpha^2 - \frac{\omega_o^4}{\omega_c^4}} \quad (10)$$

and

$$C_f = \frac{1}{R_{lm}}\sqrt{\frac{\omega_o^2}{\alpha^2\omega_c^4 - \omega_o^4}} \quad (11)$$

where R_{lm} is the maximum load of the inverter. The quantity of the formula as a function of f_{sw} for maximum ripple current α is between 20% and 40% [12].

IEEE Std. 519-1992 has set harmonic limits for voltage and current. The voltage and current of the total harmonic distortion (THD) can be obtained from the equation [13].

$$THD_V = \sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_1}} \quad (12)$$

and

$$THD_I = \sqrt{\frac{\sum_{n=2}^{\infty} I_n^2}{I_1}} \quad (13)$$

V. Simulation Results

The simulation is carried out with the PSpice A/D Lite software to test the characteristics of the filter and the overall system. Quartus Prime 18.0 Lite Edition and ModelSim are used to create and simulate algorithms from the SPWM generation system. The purpose of system simulation is to optimize the performance of the system and reduce losses before it is implemented on the hardware. The parameters of the single-phase inverter system are listed in Table I.

A. Characteristic of LC filter in single-phase inverter

This section describes the dependency of the characteristic and component values of LC filter in stand-alone inverter mode on the switching frequency (f_{sw}). The varying component values are shown in Table I. Changing f_{sw} causes the value of the filter component parameters to change according to the formula when designing the LC filter. The higher the frequency f_{sw} the smaller the value of the filter component parameters, whereby the size of the filter becomes smaller and the costs are reduced. The values in the filter parameters are listed in Table II.

TABLE I. Single-Phase Inverter Parameters.

Parameter	Value	Unit
V_{DC}	24	V
V_o	18	V
P_o	350	W
f_o	50	Hz
f_{sw}	5, 10, 15, 20, 25, 30, 40	kHz
R_{load}	300	Ω

TABLE II. Component Values for Changes in f_{sw}.

f_{sw}	Component Value		
	L_1	C_f	R_{load}
5 kHz	377 µH	617 µF	300 Ω
10 kHz	176 µH	330 µF	300 Ω
15 kHz	147 µH	175 µF	300 Ω
20 kHz	73 µH	194 µF	300 Ω
25 kHz	88 µH	104 µF	300 Ω
30 kHz	81 µH	78 µF	300 Ω
40 kHz	76 µH	46 µF	300 Ω

Fig. 5 show the output characteristics of a single-phase inverter with LC filter according to Table II. The lowest output voltage amplitude is 11.22 VAC at a switching frequency of 5 kHz and the highest output voltage amplitude is 23.26 VAC at a switching frequency of 40 kHz. This is caused by the voltage drop across the filter. Table II show where the higher switching frequency reduces the component values in the LC filter based on equations 10 and 11. As mentioned previously, the f_{sw} represents the frequency to generate a single-period sawtooth or triangle waveform. Hence, setting larger switching frequency will generate larger number of triangle waveforms, where this triangle signal is called as modulating or carrier signal.

Fig. 5 and Fig. 6 show the output voltage and THD magnitude after passing it through the LC power passive filter. The values of voltage and THD are 18.68 V and 4,72%, which is close to the desired V_o parameter, determined at switching frequency f_{sw} = 10 kHz. The THD value is below 5%, or below the limit determined by the IEEE standard 519-1992. From Fig. 6, it seems that setting larger number of modulating signals per single-phase inverter output period will increase the THD value. The THD data is obtained from PSpice simulation, where the value of the LC filter parameters is also changed according to the component values shown in Table II.

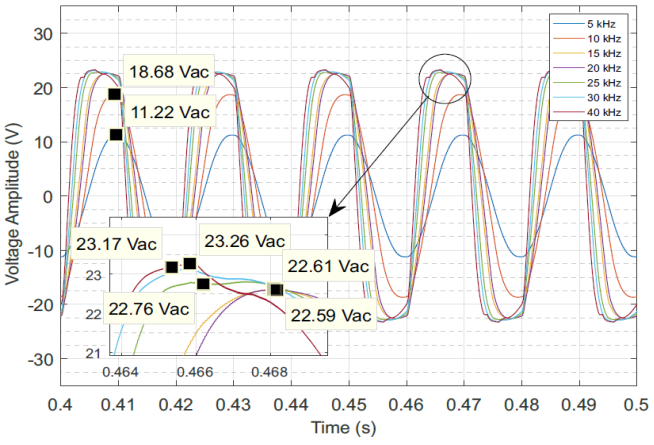


Fig. 5. The amplitude of the output voltage of the single-phase inverter changes to f_{sw}.

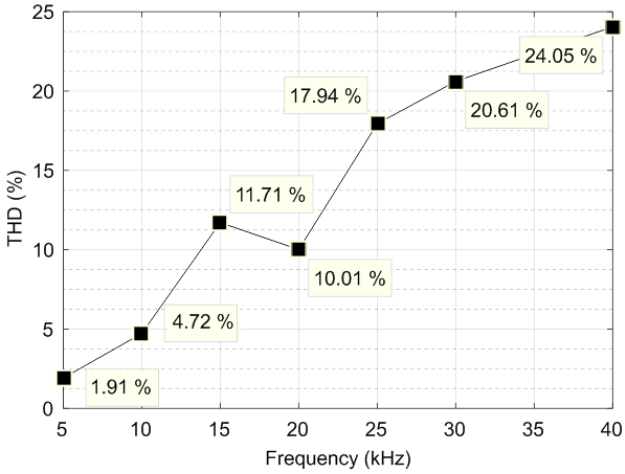


Fig. 6. Percentage of the inverter THD for varying f_{sw}.

B. *SPWM signal generator on FPGA*

The results of the modulation can be seen in the signal with the name *modulasi*, *clock_pol* is the output of the clock divider connected to the AND gate to determine the polarity of the modulated signal. *Out_mod1* is the output signal of the subsystem, *out_mod2* is the inverse of *out_mod1*. The signals at *out_mod1* and *out_mod2* are used to control the power switch of a single-phase inverter with f_{sw} = 10 kHz.

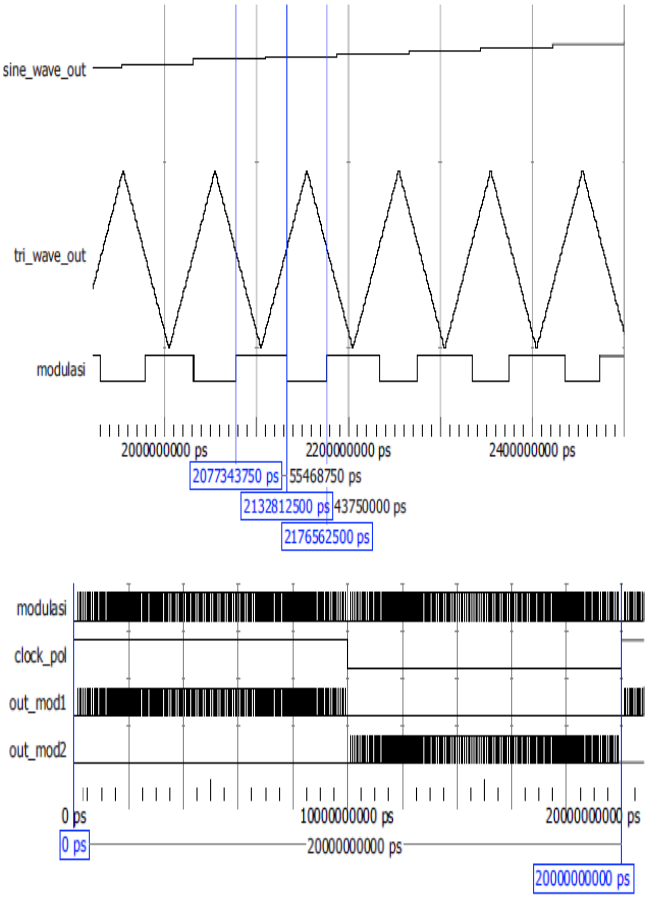


Fig. 7. Simulation of the SPWM generator power with f_{sw} = 10 kHz.

VI. Experimental Results

The simulation results obtained are then implemented by designing a single-phase inverter that is adapted to the circuit and using the pre-determined parameters. The figure shows the results of the design of the single-phase inverter with LC filter with load resistance 300 Ω / 150W. The used control device is Altera Cyclone IV EP4CE22F17C6N DE0-Nano.

Fig. 9 shows the results of measuring the output voltage of the inverter after passing it through the LC filter. With 24V DC input voltage, the amplitude of the inverter output voltage is about 23.6 V. The measurements were carried out using an oscilloscope with the calibration probe x10. On the picture you can see that it still has a fairly high harmonic interference, which is 17.71 % at the fundamental frequency of 50 Hz.

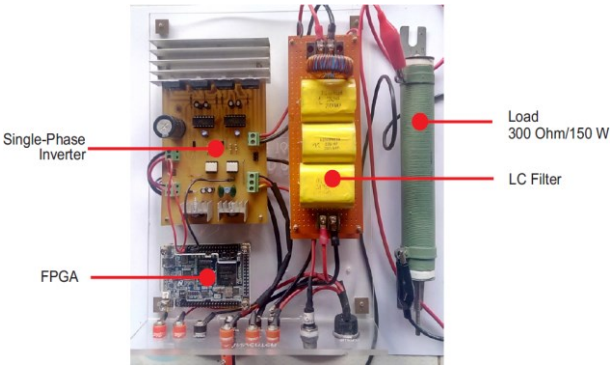
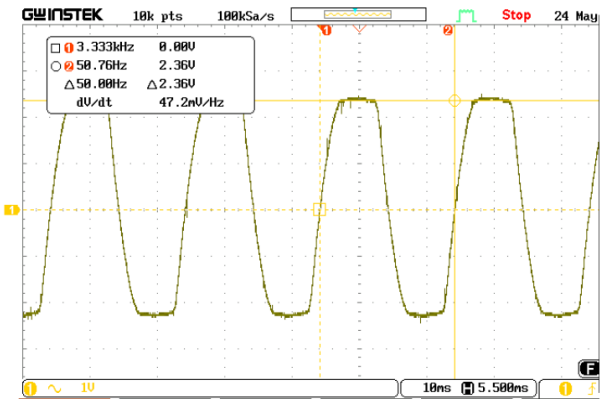
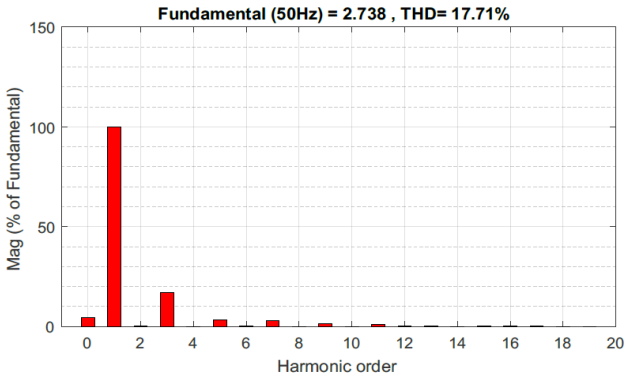


Fig. 8. Research design for single-phase inverter



(a)



(b)

Fig. 9. (a) Output voltage of the single-phase inverter with LC filter (b) the THD spectrum.

VII. Conclusions

Based on the simulation results, testing and analysis, it can be concluded the switching frequency from 5 kHz to 40 kHz affects the size and cost of the inductor and capacitor. When higher switching frequency is used, the smaller size and cost of the filter also gets a high voltage level. Developed LC filters have good attenuation with a THD of 4.72% below 5% according to the IEEE Std 519-1992 standard. It gives voltage amplitude of 18.68 V. Based on the simulation results, the system is then implemented to be a real hardware. With fundamental frequency of 50 Hz, the THD of the real hardware is about 17.71%. This THD is higher than the acceptable standard. Therefore, further work should be addressed to suppress the THD, e.g. by using other kinds of passive power filters.

The main outcome of the paper is the implementation of the PWM generator on the FPGA device. By using Cyclone IVE device with device number EP4CE22F17C6, the total logic elements (LEs) needed to implement the SPWM block is about 107 LEs out of 22,320 LEs (less than 1%) with total number of registers is 49.

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