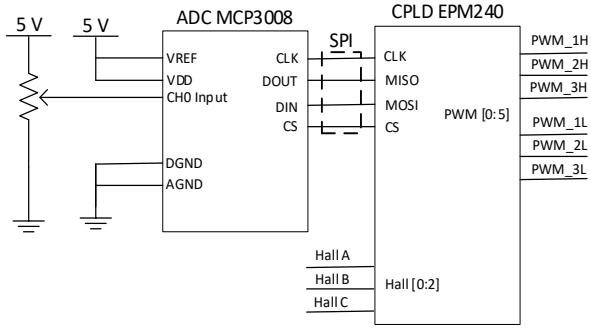
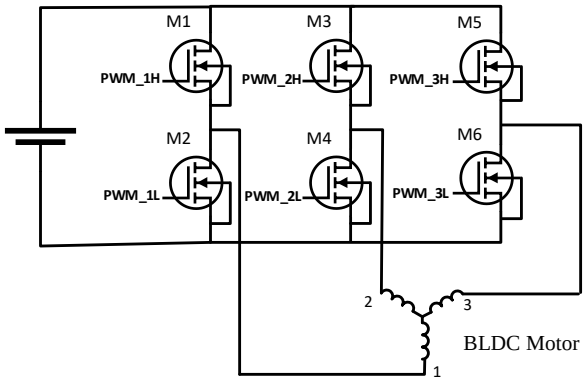
I. Implementation and Experimental Result

The simulation results verified the control algorithm according to the proposed system. Logic control was then implemented to CPLD Max II: EPM240T100C5 using JTAG via Quartus software. Figure 6 shows the logic schematic implemented to the CPLD. Total logic elements used in this design are 114 of 240 logic elements (LEs), utilize around 48% of EPM240 capability, and take 14 pins of 80 for input and output.



(a) Input and output connection



(a) 3-phase Inverter

Fig. 1. Hardware Implementation Setup.

The experimental setup is shown in Figure 1. BLDC motor used is rated for 36V and 350W, and six MOSFET is IRF3808. Hall built-in sensor on BLDC motor directly connected to CPLD through a pull-up resistor. Input signal from hall sensor is 5 volts for high logic signal and 0 volts for low logic signal. CPLD EPM240 runs at 3.3 V logic, and therefore it is needed a MOSFET driver to amplify the signal to the gate of MOSFETs. The result in Figure 2 shows the correlation between hall sensor, potentiometer value, and phase sequence. The correlation shows during full turn to 5 volts on ADC and therefore it is commutating to counterclockwise direction of 100% duty cycle. Each high side output variable duty cycle according to potentiometer, and for low side, it changes whenever hall sensor jumps to next pattern.

The testing of BLDC motor established in a condition without load and two variations with different loads. The correlations between voltage supplied into BLDC and speed of the motor are shows in Figure 3 accordingly for both directions. The reference voltage shows on figure 3 is measure during condition when hall a, b and c are 010 and measuring on winding voltage 1-2. Maximum speed achieved on no-load condition is 600 RPM, variation 1 load is 500RPM, and variation 2 load is 370 RPM. The current for no-load, variation 1 and variation 2 are around 0,76A, 1,34A, and 2,27A.

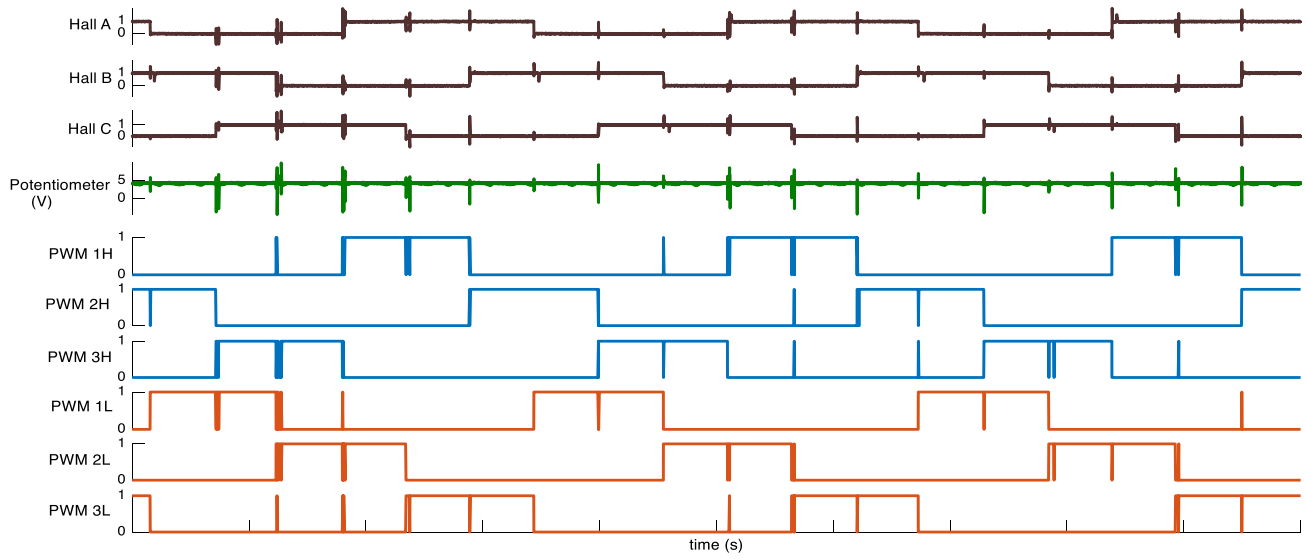


Fig. 2. BLDC control motor signals (experimental result).

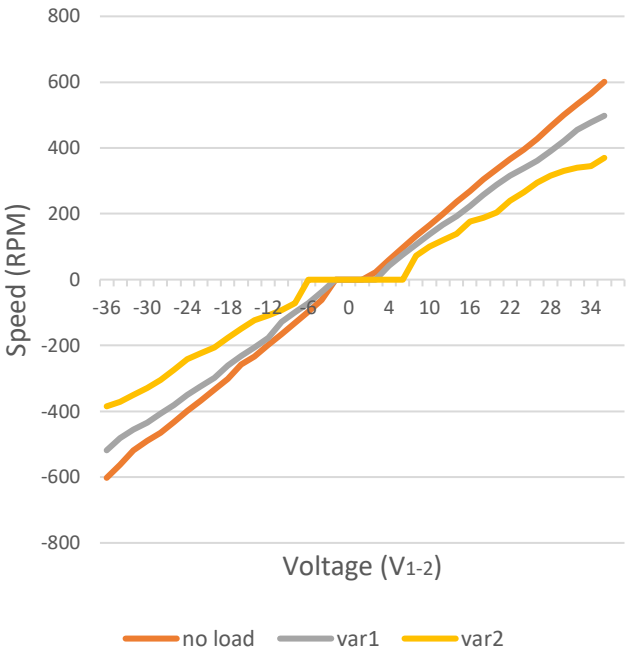


Fig. 3. Speed results on clockwise and counterclockwise direction.

II. Conclusion

In this paper, the control system of the BLDC motor using a complex programmable logic device (CPLD) is presented. The control system generates PWM signals according to six-step commutation using hall sensors. BLDC motor speed control is achieved by varying duty cycles of PWM with a frequency 20KHz. Duty cycle controlled with comparing ADC value from a potentiometer and compare with an internal counter. The control system was created with Verilog HDL and simulated using Modelsim-Altera. The algorithm implemented to CPLD Max II: EPM240T100C5 with total logic elements (LEs) is about 114 out of 240, around 48% of EPM240 capability, and takes 14 pins for input and output for the overall system.