FPGA-Based Electronic Pulse Generator for Single-Phase DC/AC Inverter

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***Abstract*—This paper is focused on the development of a signal generator *Sinusodal Pulse Width Modulation* (SPWM) which is used to control a full wave power switch on a single phase inverter based on a *Field Gate Array Programmable* (FPGA). FPGA can operate in parallel with quite high computing capabilities. Quartus Prime 18.0 Lite Edition and ModelSim are software used to describe and simulate SPWM generating units. The digital signal generator of sine and triangle signals with the Look Up Table (LUT) method which is stored in FPGA internal memory. Mosfet IRFP460 is used as a semiconductor switch on a single phase inverter with a full brige configuration. The system is first simulated using PSpice A / D Lite before being tested on a single phase inverter device.**

***Index Terms*—IRFP460, Inverter, FPGA, Full brige, SPWM, Look Up Table**

I. INTRODUCTION

Renewable energy is an energy source that is environmentally friendly and able to produce the amount of power that is large enough to meet the needs of consumers [1] [9]. One of the promising and renewable energy source systems as a topic of research lately is photovoltaic systems [8]. Inverters as an important part in converting energy sources Direct current (DC) to renewable energy into alternating current (AC) to be used by home or industrial scale consumers,as shown in figure 1.

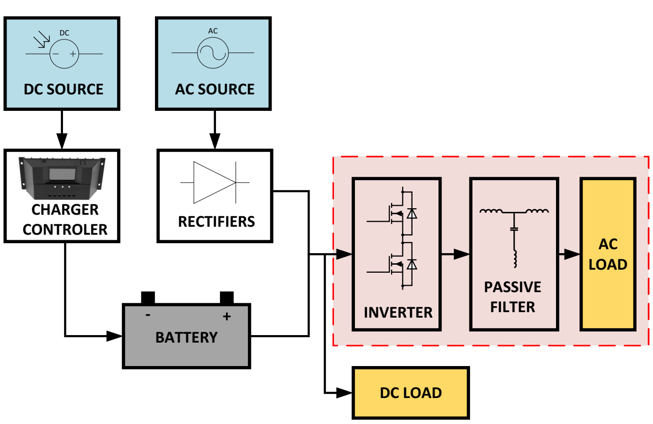

Fig. 1. Diagram of solar power generation system

Several previous studie were carried out to improve the performance of the system on the inverter so that it obtained the ideal performance. Modulation technique is one way to adjust the inverter to get inverter output with low and efficient harmonic distortion. The sinusoidal pulse width modulation technique (SPWM) is one of the modulation techniques that is widely used in inverters to control semiconductor switches by comparing the reference and career waves. SPWM can be generated digitally using Field Programmable Gate Array (FPGA). The advantages in the wave generation process with digital methods are not affected by noise [2]. FPGA has several advantages in terms of process speed, flexibility, small power consumption and reduced circuit size because it can work in parallel [3] [4]. Look Up Table (LUT) is used to present digital and triangular waves digitally, LUT sample data is then stored in internal memory. The method other than LUT is by making an SPWM output wave by using the time sample ON and OFF without having to generate a sine wave and a triangle on the FPGA [5] [6].

This study focused on the SPWM generator control unit based Altera Cyclone IV EP4CE22F17C6N on a single phase inverter with a full-brige semiconductor switch configuration using Mosfet IRF460. The design of the SPWM generator unit system uses Quartus Prime 18.0 Lite Edition and ModelSim software. Overall simulation of a single phase inverter system using PSpice A / D Lite.

II. SYSTEM DESCRIPTION

A. Single Phase Inverter System

This research uses a full brige configuration with mosfet IRF460 as a semiconductor switch. Large capacitors are used to maintain voltage. Operation of a semiconductor switch cannot be operated on the same arm to avoid short circuit in the circuit [7]. Semiconductor switch control uses SPWM techniques that are digitally generated with FPGA devices.

The M_1 and M_2 semiconductor switches are in the "High" condition simultaneously, M_3 and M_4 have opposite conditions "Low" and vice versa. The output of the full bridge inverter is basically in the form of a square wave which is generated from the semiconductor switching process and have high harmonic value.

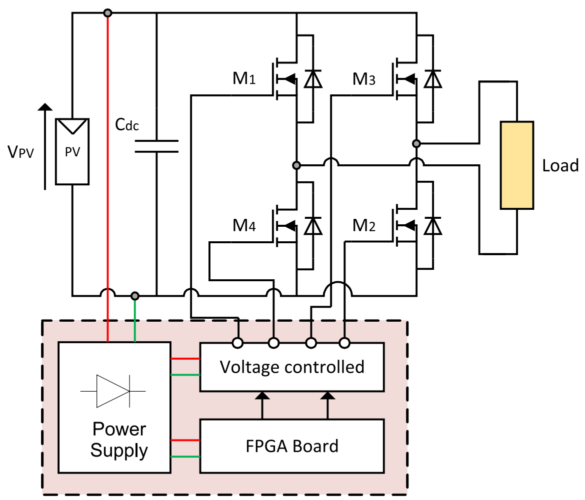

Fig. 2. Inverter model

B. Sine and Triangle Digital Signals

As previously explained the generation of sine and triangular waves can be done by sampling with the Look Up Table (LUT) method. In this case the sinusodal wave is copied 256 times so that for the half wave 128 samples and the triangular wave 128 times sampling.

$$v_c(t) = V_m sin(\frac{2\pi t}{n}) \tag{1}$$

$$v_{\triangle}(t) = \frac{V_m t}{n} \tag{2}$$

V_m is the voltage amplitude and n number of sampling. Whereas for modulation index magnitude can be obtained by equation [7].

$$m_a = \frac{v_c}{v_{\triangle}} \tag{3}$$

The greater the number of sampling the more thoroughly the quantization and encoding process as shown in the figure 3. The discrete value obtained is then inserted into the internal data memory with the bit quantities adjusted for the amplitude voltage values for each signal. The pulse width of T_{on} and T_{off} the square wave of SPWM are generated from the modulation process between the triangle $v_{\triangle}$ and Sine v_c signals.

C. SPWM Signal Generator Design

SPWM is generated using the Altera Cyclone IV EP4CE22F17C6N DE0-Nano device with the LUT method. The SPWM signal generator is basically the result of a comparison of the modulation of the triangle $v_{\triangle}$ and sine v_c waves which is an analog waveform. Because FPGA devices work digitally, triangular waves and sine waves are represented digitally by sampling.

Altera Cyclone IV EP4CE22F17C6N DE0-Nano has an internal oscillator of 50 MHz, to generate a frequency scale

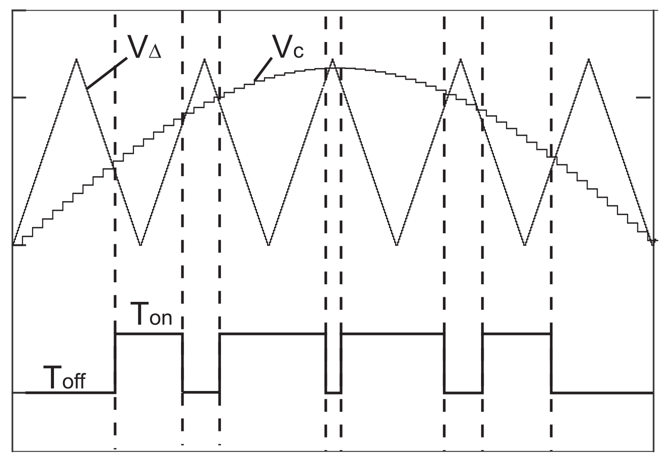

Fig. 3. Illustration of Sine and Triangle Digital Signals

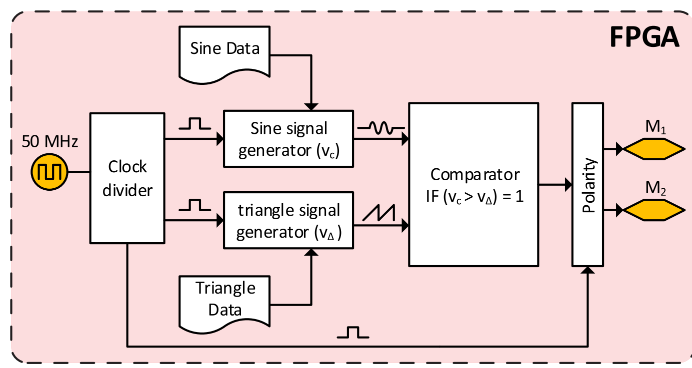

Fig. 4. Algorithm single phase SPWM signal generator

that suits your needs then it requires a frequency divider unit. The N-bit counter is used to count when taking triangle signal and sine data stored in internal memory. The comparison unit works comparing the value of the sine signal data which has been multiplied by the modulation index value in the multiplier unit with a triangle signal, So as to produce pulse width according to the results of the comparison of the two signals. The polarity unit functions to produce half a wave of 50 Hz of the desired frequency to avoid the occurrence of ON conditions simultaneously on both mosfet M_1 and M_3 which have the opposite ON state.

III. SIMULATION RESULTS

Simulation is done using PSpice A/D Lite software based on predetermined parameters. Simulation also aims to evaluate system design by knowing the characteristics of the system to be implemented and can reduce the possibility of failure so that it can optimize system performance.

A. Simulation of SPWM Signal Generating System on FPGA

FPGA as a device used to control semiconductor power switches using the VHDL or Verilog description language. System design uses Quartus Prime 18.0 Lite Edition and

ModelSim software. Sine and triangular wave data is generated using the LUT method is stored in the internal memory will then be called in accordance with a predetermined order. Frequency dividers are used to determine the amount you want to use based on the number of samples 256 times. *Sine* is generated with a frequency of 50 Hz. whereas, *Triangle* is generated with a frequency of 1 kHz and the modulation index specified is 0.9375 as shown in the figure 5. *Comp* is the result of *sine* and *triangle* modulation waves. Output M1 is generated from the *Comp* wave multiply by *Polarty*, M_3 is the inverse of M_1.

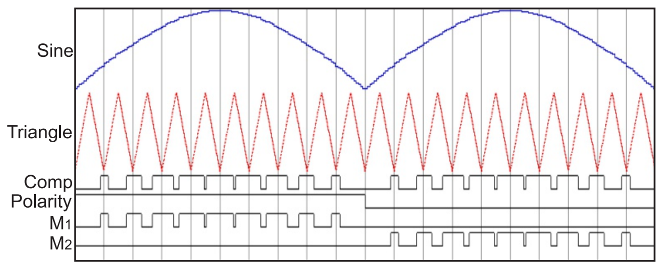

Fig. 5. Output of the SPWM generator system using FPGA

B. Simulation of Single Phase Inverters with FPGA Unit Control

The overall single phase inverter simulation is done using Pspice AD Lite software. Figure 6 shows the results of the simulation of the output of a single phase inverter with a Resistor 220Ω and a voltage amplitude of 20 V_{ac}.

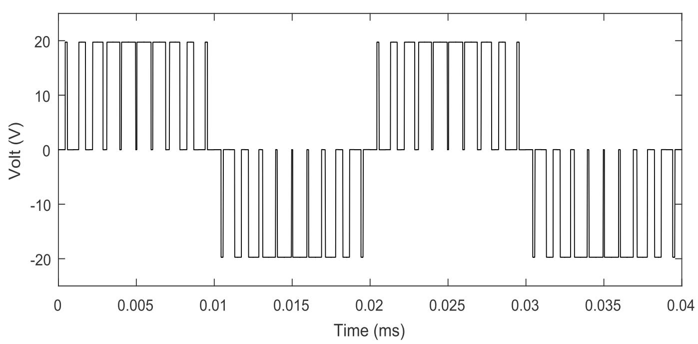

Fig. 6. Simulation of Single Phase Inverter Output with Resistor Load

IV. EXPERIMENT RESULTS

The experiment was carried out based on simulation data, the main controller uses Altera Cyclone IV EP4CE22F17C6N FPGA DE0-Nano with a 50 MHz oscillator frequency. Bipolar switching frequency is 1kHz with a fundamental frequency of 50Hz. Single phase DC-AC inverter experiments using the H-Bridge configuration consisting of four Mosfet IRFP460 semiconductor components. Power supply is used to supply the voltage on the FPGA and Voltage Controlled with the required voltage level. The FPGA requires a 3.3 V_{dc} voltage to operate properly while the Voltage control requires a voltage of 18 V_{dc} according to the requirements of the IC TLP250 and IR2110. Voltage control circuit consists of two components IC TLP250 and IR2110 to meet the gate input voltage on the mosfet IRFP460 with a supply of 18 V_{dc} with a maximum voltage of $\pm 30 V_{dc}$. The high and low output signals from TLP250 are then reprocessed by IR2110 to produce the high and low sides used to control M1 and M3. IR2110 uses two pieces to control both arms in the H-brige Mosfet configuration. Measurement of a single phase inverter circuit using an oscilloscope.

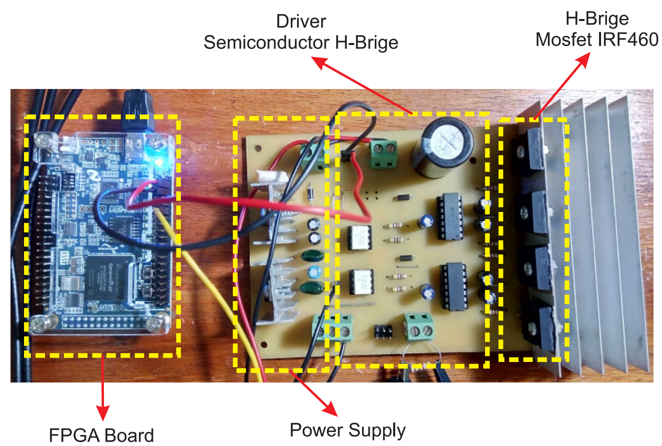

Fig. 7. Single phase inverter device

Figure 8(a) shows the output wave generated by the FPGA Board with a voltage of 3.3 V_{dc} with a 1 V_{dc} Probe x1 scale osciloscope calibration. The full Brige configuration requires four signals that control M_1, M_2, M_3 and M_4.

Figure 8(b) shows the output of the IC TLP250 with four output signals to control semiconductor switches alternately M_1, M_2 (ON) and M_3, M_4 (OFF) and vice versa to avoid short circuit with 2 Vdc Probe x10 scale osciloscope calibration.

Figure 9 shows the inverter output with a 10 V scale calibration and probe x1. The results obtained by the 18 V_{ac} voltage amplitude with Resistor load and fundamental frequency of 50 Hz with switching frequency of 1 kHz. The output wave is still in the form of a square wave because no filter has been added.

V. CONCLUSION

This experiment presents a SPWM control unit using FPGA with a flexible structure and can be adapted to a single phase dc / ac inverter. The simulation results using ModelSim show that the design of FPGA-based SPWM generator systems has been successful. The LUT method for presenting analog waves into digital with a switching frequency of 1 kHz and a fundamental frequency of 50 Hz. Clock divider regulates the processing time of LUT data samples to reach a predetermined frequency. The SPWM generator unit system is then tested using the Pspice A / D Lite Software with the result of a 20 V_{ac} Amplitude voltage and a frequency of 50 Hz. The inverter system design is then implemented on a single phase inverter

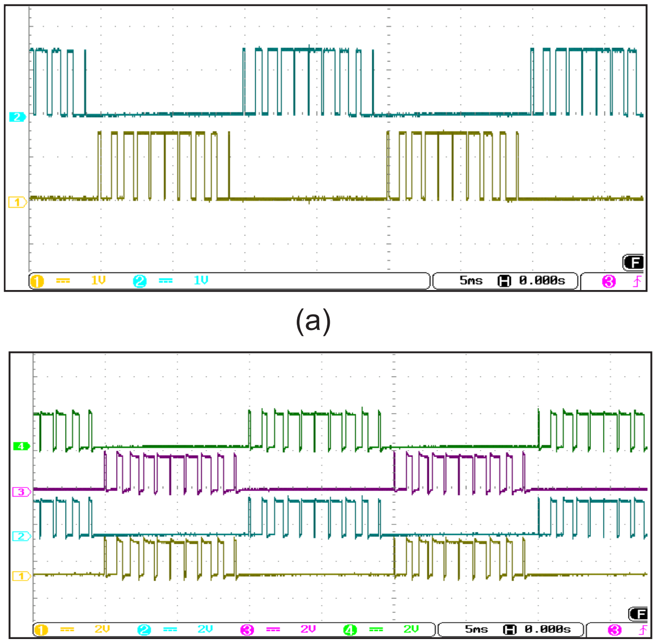

Fig. 8. (a) FPGA output (b) Output of TLP250 Optocoupler

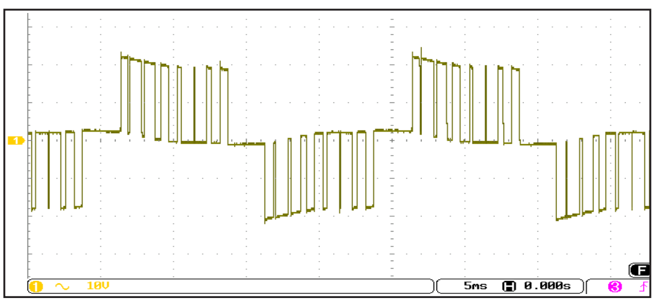

Fig. 9. Single Phase Inverter Output

prototype with a resistor load, the measurement results using oscilscope show an amplitude of output voltage 19 V_{ac} with a switching frequency of 1 kHz and a fundamental frequency of 50 Hz.

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REFERENCES

[1] Sunita, S. Budhiraja, J. Singh and D. Bhat, "FPGA based photovoltaic (PV) inverter with SPWM algorithm for photovoltaic system," 2016 5th International Conference on Wireless Networks and Embedded Systems (WECON), Rajpura, 2016, pp. 1-5.

[2] T. Sutikno, N. R. N. Idris, I. M. Alsofyani, A. Jidin and L. L. Raj, "FPGA based five-phase sinusoidal PWM generator," 2012 IEEE International Conference on Power and Energy (PECon), Kota Kinabalu, 2012, pp. 314-318.

[3] A. Agarwal, V. Agarwal and I. A. Khan, "FPGA based Sinusoidal pulse width modulated frequency converter," 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, 2016, pp. 1-7.

[4] M. Lakka, E. Koutroulis and A. Dollas, "Development of an FPGA-Based SPWM Generator for High Switching Frequency DC/AC Inverters," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 356-365, Jan. 2014.

[5] A. B. Afarulrazi, M. Zarafi, W. M. Utomo and A. Zar, "FPGA implementation of Unipolar SPWM for single phase inverter," 2010 International Conference on Computer Applications and Industrial Electronics, Kuala Lumpur, 2010, pp. 671-676.

[6] Isa, Mohd Nazrin Md, et al. "FPGA based SPWM bridge inverter." American Journal of Applied Sciences 4.8 (2007): 584-586.

[7] RASHID, Muhammad H., et al. Power electronics handbook: devices, circuits, and applications/edited by Muhammad H. Rashid. 2011.

[8] F. A. Samman and A. Azhari, "DC/AC power converter for home scale electricity systems powered by renewable energy," 2016

[9] International Conference on Smart Green Technology in Electrical and Information Systems (ICSGTEIS), Bali, 2016, pp. 149-154. F. Sevilmi and H. Karaca, "An Experimental Study of Grid Tied Inverter for Renewable Energy Systems," 2018 International Conference on Smart Energy Systems and Technologies (SEST), Sevilla, 2018, pp. 1-6.