FUZZY LOGIC IN THE PHASE-LOCKED LOOP DC MOTOR SPEED CONTROL SYSTEM

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Abstract - This paper presents a novel design using fuzzy logic control and phase-locked loop to obtain a DC motor speed control system with excellent regulation and high robustness . The fuzzy logic controller is incorporated in order to achieve quick control of motor speed smo0thly. The fuzzy logic controller enhances the robustness of the motor control system , which can handle abrupt load variation and exhibit good disturbance behavior. The PLL becomes effective at steady-state conditions when the speed error is small . A control scheme using fuzzy control of DC motor speed with extremely accuracy provided by PLL is implemented. Simulation demonstrates the effectiveness of the proposed scheme. Test results show that a system which consists of both fuzzy control and PLL can yield a high performance DC motor speed control system .

I. INTRODUCTION

Phased-locked loop (PLL) techniques have wide applications in systems where exact frequency synchronization is required. This technique has also been applied to the speed control of DC motors , where motor speed can be locked to an accurate reference frequency[1-5]. The resulting motor speed will not drift due to environmental changes. The speed accuracy of 0.002% for a PLL-controlled DC motor system has been achieved [1]. However , PLL-controlled motor drives have the following shortcomings.

(1) PLL-controlled motor systems tend to be unstable for low-speed operation [2].
(2) PLL-controlled motor systems have large response time.
(3) PLL-controlled motor systems may get out of synchronization for an abrupt load variation [4].
(4) The system may be rejected to get into PLL operation mode , so that PLL cannot start operating smoothly.

To overcome the disadvantages of PLL motor control system, a PC-based fuzzy logic controller (FLC) is incorporated for combination with phase-locked loop for precise and robust speed control of a DC motor. Fuzzy logic enables the use of empirical experience in a control system design. The benefits of using fuzzy logic controller in control system have been demonstrated in a variety of applications [6-10]. The fuzzy logic controller is used to pull the motor speed into the locking range of PLL . When the speed error between the setpoint speed and the measured motor speed is larger than a preset value , the motor is incremented or decremented by the fuzzy logic controller toward the PLL locking range. In order to achieve excellent speed regulation , PLL control replaces the FLC when speed error is within the locking range of the PLL. When the system operates in the phase-locked loop , the speed of the motor is locked by a reference frequency. Synchronization of the motor speed to a very accurate reference frequency warrants that the motor speed will not drift due to temperature or component wear. Thus , a precise speed control of DC motor operation is achieved.

II. SYSTEM CONFIGURATION

The block diagram of the PLL-controlled DC motor speed drive incorporating FLC is illustrated in Fig. 1. A power amplifier is used to provide a DC voltage with adequate power to drive the DC motor at the desired speed. An encoder mounted on motor shaft serves as a speed feedback. The PLL or FLC is employed to control the DC motor speed. When speed error is larger than the preset value, the FLC is active. Thus, motor speed is accelerated or decelerated toward the setpoint speed through fuzzy control.

The system flowchart is shown in Fig. 2. When motor speed error reaches the PLL locking range, the system enters the PLL operation. Once the speed error is beyond the preset range, the system will return to the fuzzy logic control mode. The operation mode is selected by the switching logic as illustrated in Fig. 1.

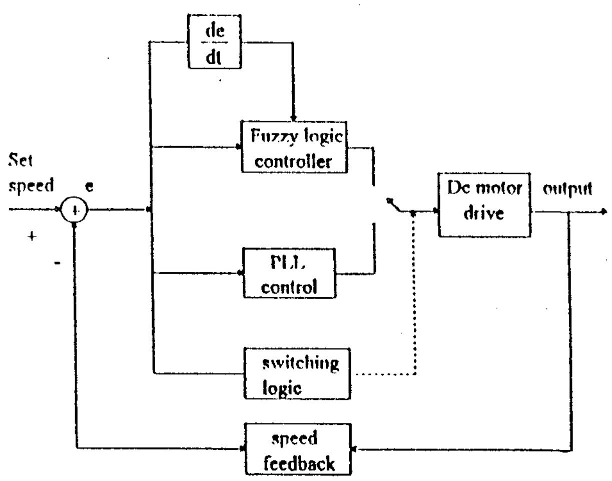


Fig. 1 Block diagram of DC motor speed control system

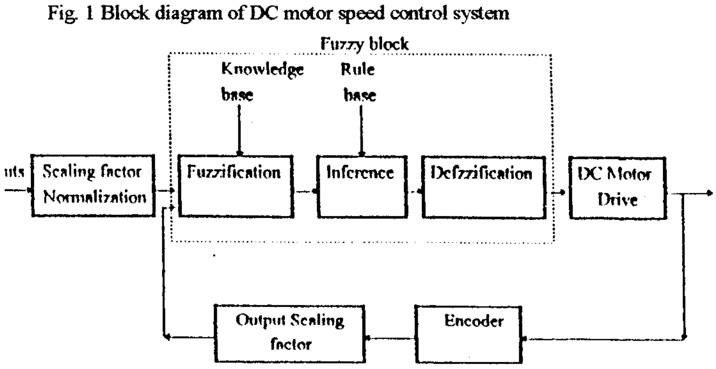


Fig. 3 Fuzzy logic controller in a DC motor speed control system

III. FUZZY LOGIC CONTROLLER

The main benefit of using fuzzy logic design in DC motor speed control system is that the same controller can easily be applied to various motors having different parameters. The function of FLC is to achieve quick speed response without overshoot and to provide good disturbance behavior.

The block diagram of the fuzzy logic controller is shown in Fig. 3. The knowledge base consists of input and output membership functions. The rule base is made up of a set of linguistic rules relating the fuzzy input variables to the desired fuzzy control actions. Fuzzification converts a crisp input signal into fuzzified signals that can be identified by their degrees of membership functions. The inference mechanism uses linguistic rules to convert the input conditions into a fuzzified output. Defuzzification converts the fuzzy output into crisp controlling signals, which is the dc voltage variations (Δ v) that change the DC motor speed.

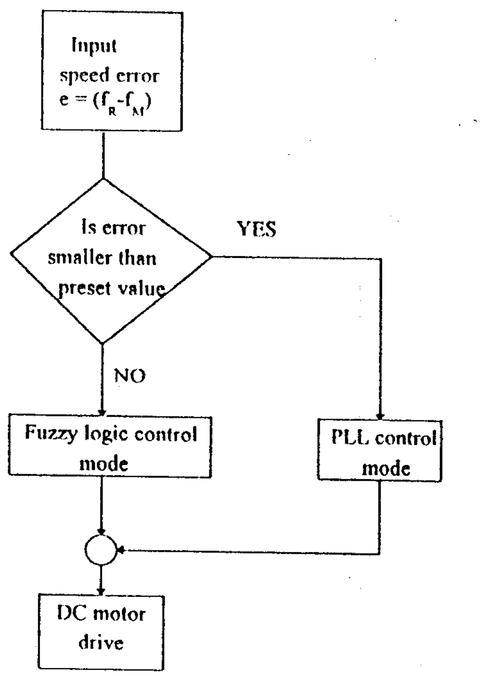


Fig. 2 Flowchart

Fuzzification maps the process error, and change of error to the fuzzy sets labels. The scaling and quantization procedure defines the range of values that characterize membership functions. The quantization of e and Δ e are shown in Table 1.

These quantized inputs are then converted into suitable linguistic labels. In this paper, the following linguistic labels are employed.

1. Input variables:

   P (positive), N (negative), Z (zero).

2. Output variables:

   PB (positive big), PS (positive small), ZO (zero). NS (negative small), NB (negative big).

The normalized membership function of input variables is illustrated in Fig. 4.

Table 1 Quantized levels for input and output variables

e (RPM)	Δe	Δv (volts)	quantized levels
-36	-60	-6	-6
-30	-50	-5	-5
-24	-40	-4	-4
-18	-30	-3	-3
-12	-20	-2	-2
-6	-10	-1	-1
0	0	0	0
6	10	1	1
12	20	2	2
18	30	3	3
24	40	4	4
30	50	5	5
36	60	6	6

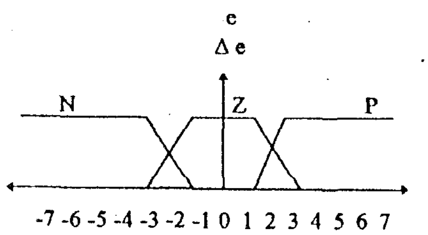


Fig. 4 Membership functions for input variables.

The rule base defines the rules which represents desired relationship between the input and output variables in terms of membership functions. The control statements are represented as a set of IF... THEN rules. The control rules used in our system are shown in Table 2. For example, a fuzzy rule can be expressed as follows : IF the speed error is negative (N) and the error change is positive (P), THEN the voltage variation driving the DC motor is positive small (PS).

The control rules are evaluated by an inference mechanism. During the rule evaluation process , the combination of the selected rules in the knowledge base can be evaluated according to any of the following methods, the min-max algorithm,the correlation-product method, and the Mamdani algorithm. An inference strategy based on the Mamdani method is used in this paper.

The membership function of the output variable (Δ v) are depicted in Fig. 5.

Table 2 Control rules

Δe \ e	N	Z	P
N	NB	NB	NS
Z	NS	ZO	PS
P	PS	PB	PB

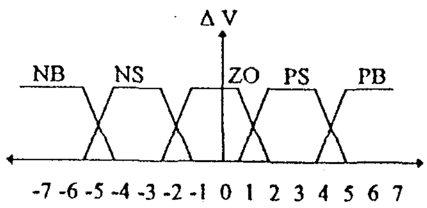


Fig. 5 Membership functions for output variables

The defuzzification process is used to determine a crisp value according to the fuzzy output from inference mechanism. Several defzzification techniques, such as weighted-average criterion, mean of maximum, and center-of-area methods are available. The center-or-area method, which computes the center of area of the inference mechanism output possibility distribution, is used as a defuzzification strategy in our system.

Based on membership function and linguistic control rules, a look-up table can be derived according to the selected fuzzification and defuzzification functions. By proper scaling, the look-up table for FLC can be obtained as shown in Table 3.

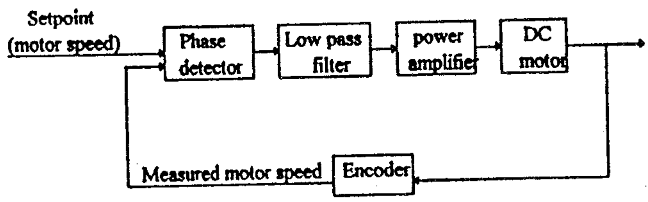
IV. PLL-CONTROLLED OPERATION

The block diagram of the DC motor drive system operating in PLL mode is shown in Fig. 6(a). which comprises a phase detector (PD), a low-pass filter (LPF), a power amplifier, a DC motor, and an incremental encoder. DC motor and encoder are used as a VCO block in the phase-locked loop.

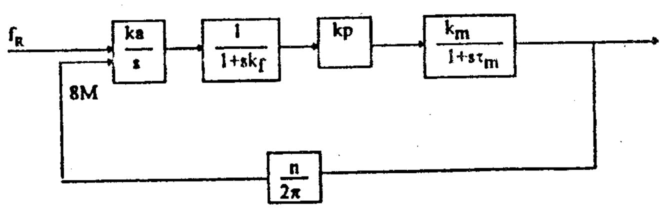
In order to analyze the stability of PLL system in Fig. 6(a), a transfer function model is developed. The modeling of the phase-locked loop system is shown is Fig. 6(b). The transfer function of the encoder is represented by $H(s) = n/2\pi$. The continuous model for the phase detector can be represented by K_d/s [2], where K_d is the constant of PD. The transfer function of low pass filter is denoted by $1/(1+s K_f)$, where K_f is the RC time constant. The power amplifier is represented by a constant gain K_p. The DC motor can be modeled by $km/(1 + \tau_m)$, where K_m is motor voltage constant and τ_m is motor mechanical time constant [5].

The model in Fig. 6(b) can be simplified to a model with forward gain G(s) and feedback gain H(s). To investigate the stability of the closed loop system, the bilinear transformation is applied. The stability can obtained using Routh-Hurwitz criteria

It can be observed from the above analysis that various design parameters can affect PLL system stability. The system designer may use the above model as a guideline for the selection of suitable parameters.



(a)



(b)

Fig. 6 Phase-locked loop DC motor speed control system.

(a) block diagram

(b) system modeling

VI. EXPERIMENTAL RESULTS

The complete PC-based DC motor speed control system using the proposed FLC and PLL is implemented to verify the theoretical analysis. The host computer is a PC 586 system. Additional interface boards are used and plugged in the PC system . These include D/A converter board , counter board , and I/O interface board . The experimental set-up is shown Fig. 7.

A 2-channel incremental encoder mounted on the motor shaft converts motor rotation into 500 pulses per turn . The pulse output from doubling circuit with 1000 pulses each turn is applied to the input of the PD and also to the counter for the measurement of the motor speed by the microcomputer .

A DC motor having the following characteristics is used for experiment : rated voltage = 24 V ,rated current = 1.1A , rated speed = 1640 rpm, $\tau_m=2$ seconds , K_d =2V/rad, Km=10 rad /sec. Other parameters are as follows : n=1000 for encoder and doubling circuit , Kd = 2V/rad for PD, and K_f =7.5 seconds for LPF.

The fuzzy controller algorithm is implemented in the PC by C language . The actual motor speed is measured at the fixed interval and speed errors are computed by PC.

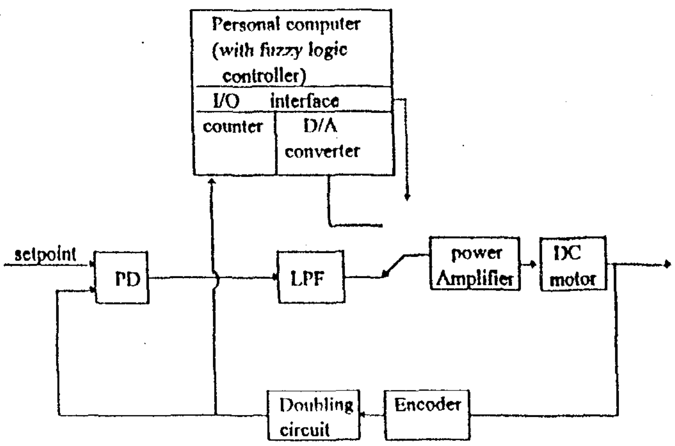


Fig. 7 Experimental set-up

For comparison , a PID control is implemented by software in PC where the FLC algorithm is realized . The experiments verify that, in comparison with pure PLL and PID control, the system with both PLL and FLC control modes provides best performance .

VII. CONCLUSION

A fuzzy logic controller in combination with PLL control to obtain a robust and precise speed control for a DC motor drive has been presented.

Conventional speed controller for DC motor system requires a complete mathematical model of the motor. Fuzzy logic design uses linguistic description to replace the mathematical model. This can reduce design complexity and expedite the development cycle. However, fuzzy control alone cannot provide best performance of DC mode speed control both in transient state and steady state . The overshoot phenomena may occur depends on the quantization levels of input and output variables . Thus the PLL control is used to replace the FLC once the speed error is within a preset limit . When the speed error is larger, the FLC becomes active and the system responds quickly by drawing the motor speed into the preset speed error range . The feasibility of using both PLL and FLC in DC motor speed control system has been demonstrated . Precise speed regulation is achieved by PLL operation . The system can quickly recover from loss of lock situation by FLC. The proposed control scheme with PLL and FLC in parallel combine the rapidity of fuzzy controller during the transient state and the accuracy of PLL control during the steady state .

It has been shown by experiment that the performance of a PLL- controlled motor speed drive improved with the incorporation of fuzzy logic controller in the system.

VII. REFERENCES

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